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MS-7808 ATX Ver:2.0

Intel -MahoBay plamform B75

CPU:

IVY bridge LGA1155

Onboard Chip:

Audio Codec: 887

LAN : RTL8111E (colay8105E)

SIO : Fintek F71878AD(colayF71868AD)

Flash ROM: SPI 128 MB

System Chipset:

Panther Point B75

Main Memory:

DDRIII (1066/1333/1600MHz)
* 2 (Dual Channel)

ACPI:

UPI

Expansion Slots:

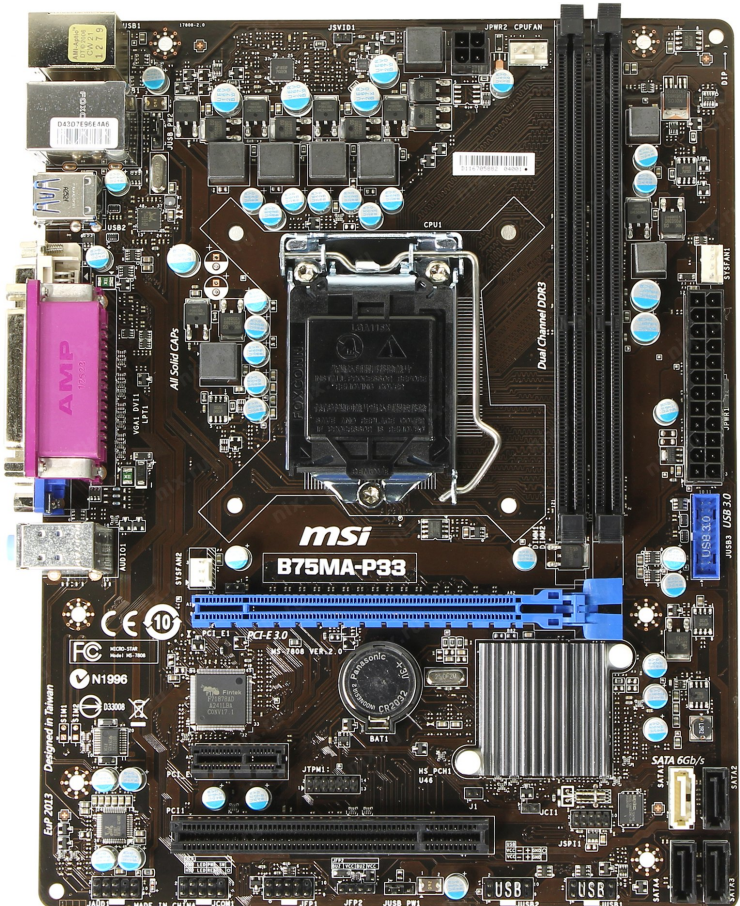
PCI Express (X16) Slot * 1
PCI Express (X1) Slot * 1
PCI Slot * 1

PWM:

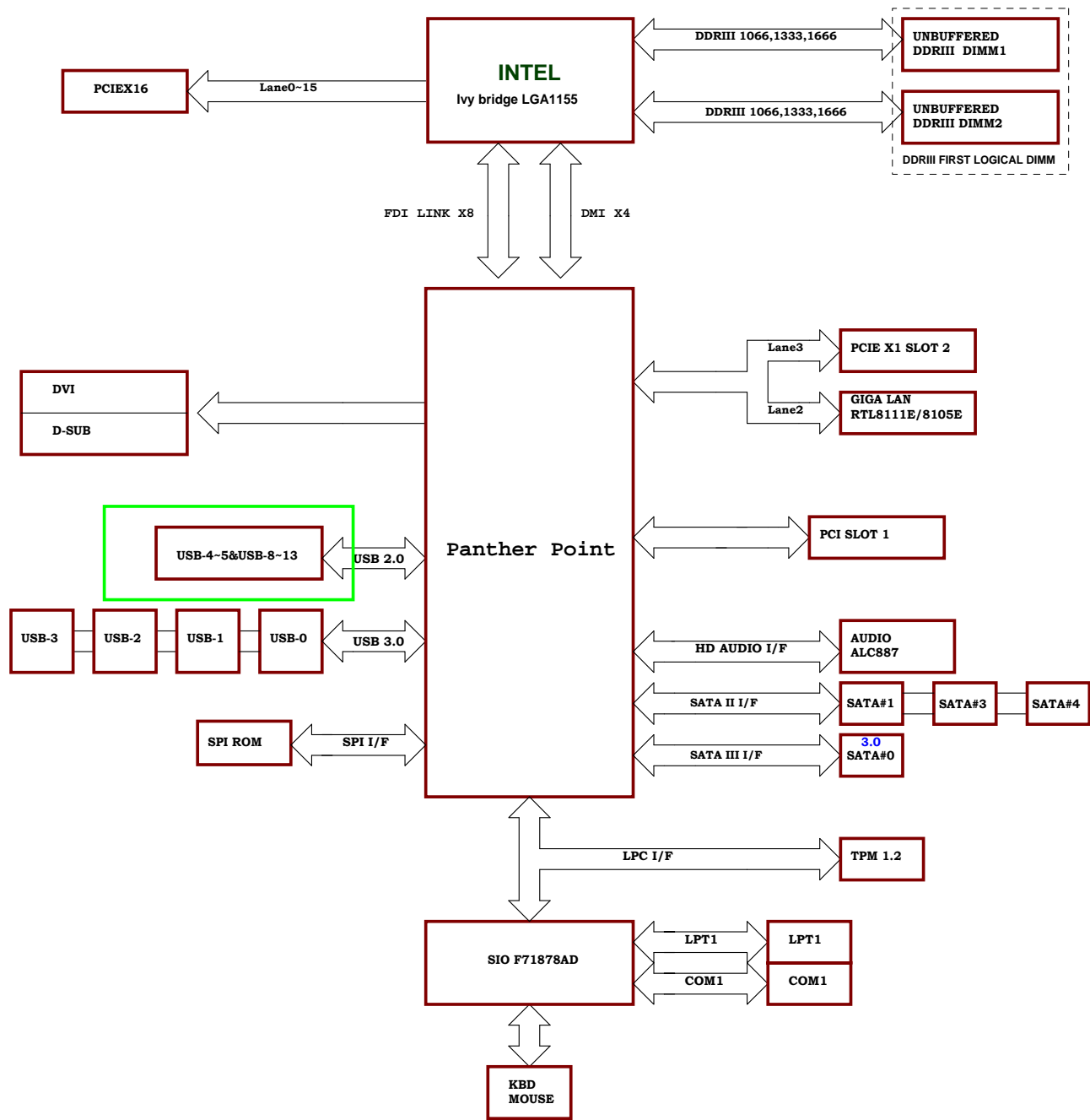
VRD12 -UT501 3+1 Phase

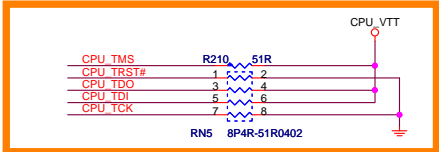
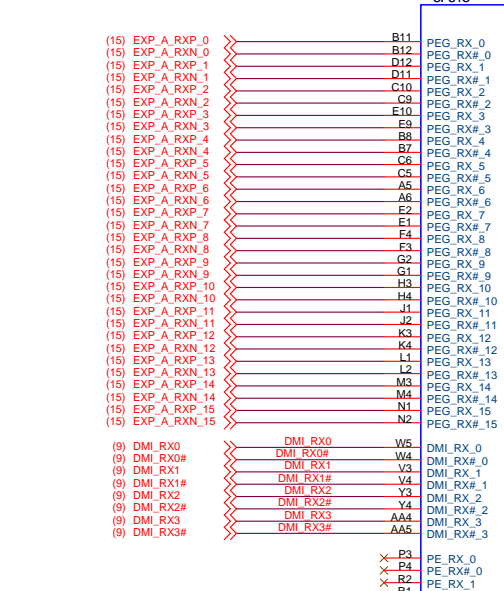
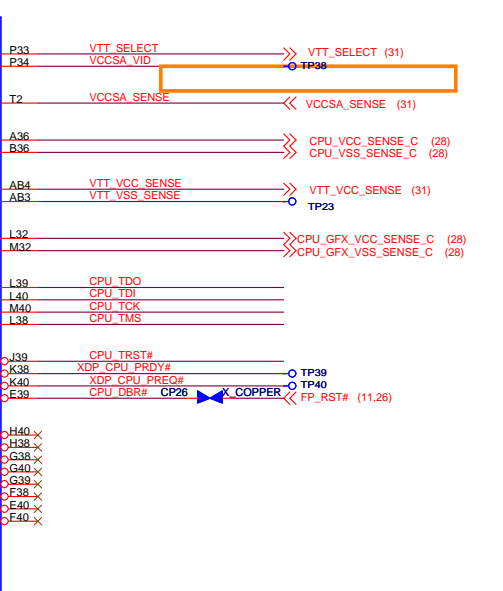
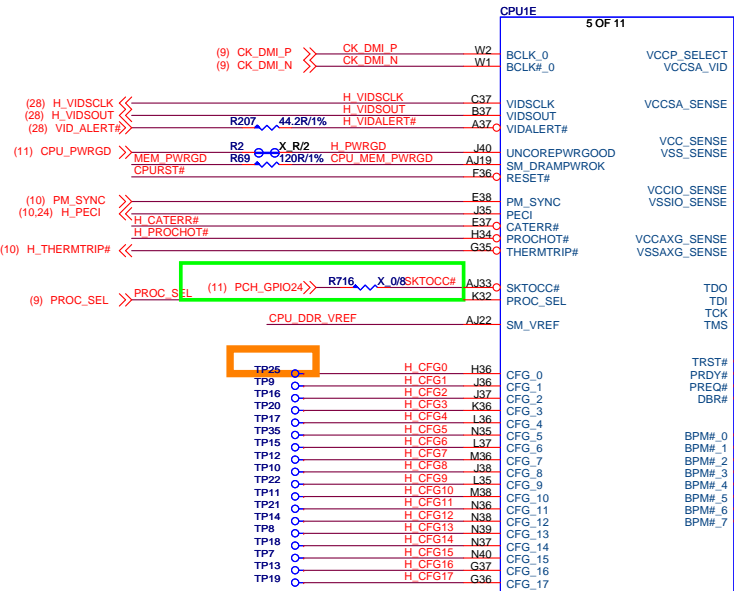
Other:

SATA3.0 x1+SATA2.0 x3 (PCH)
USB2.0 *8
REAL USB3.0 *2
FRONT USB3.0 *2

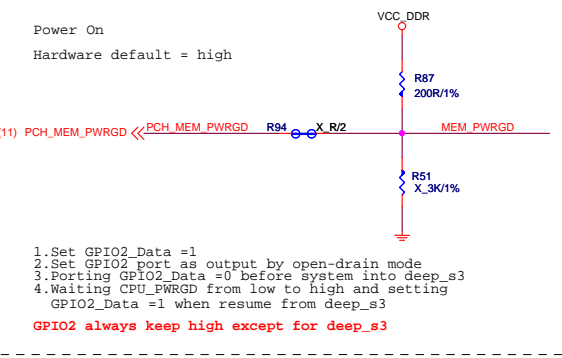
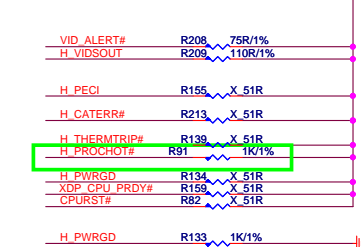


MS-7808 Block Diagram

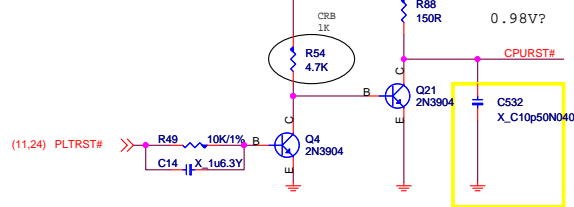


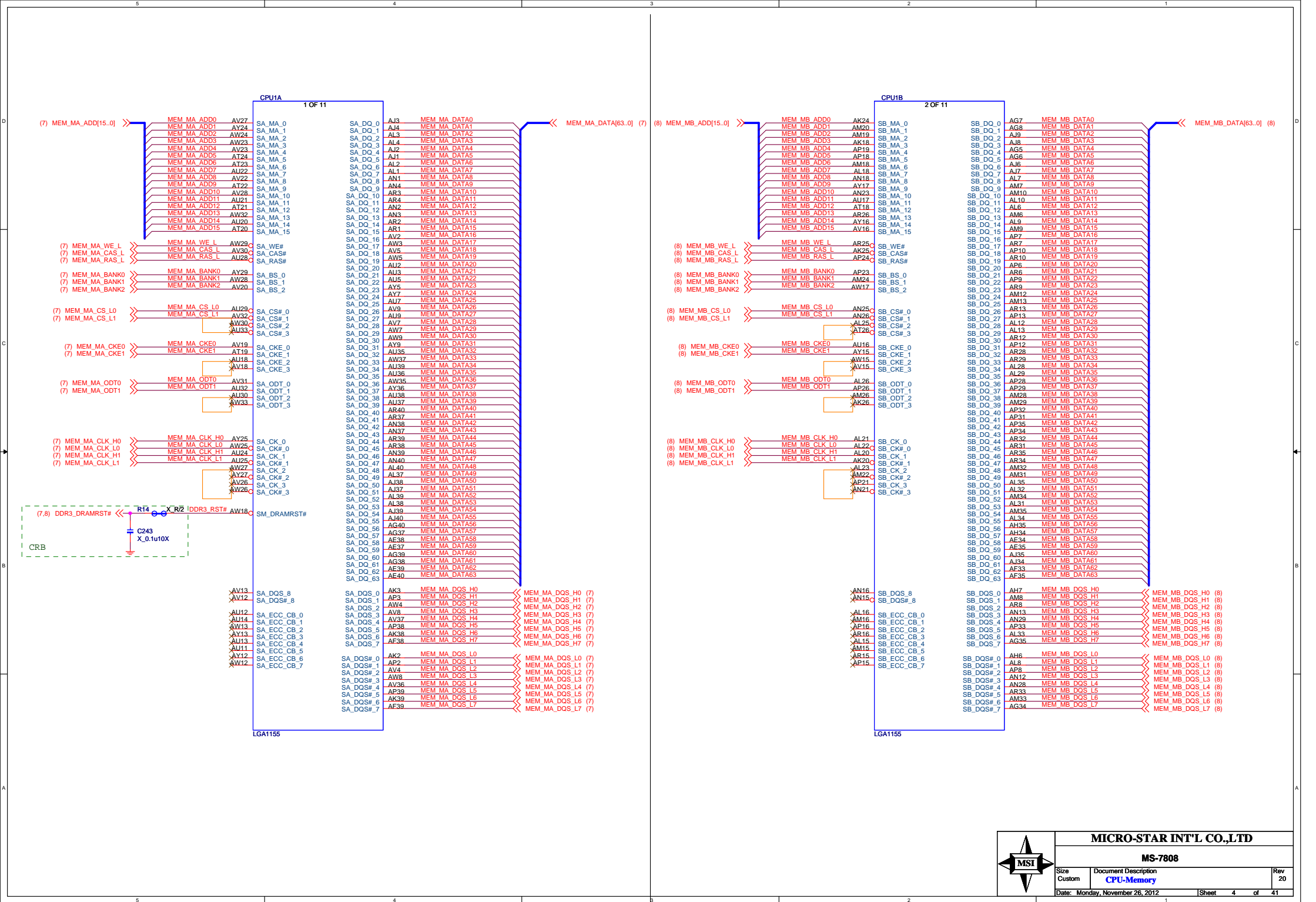


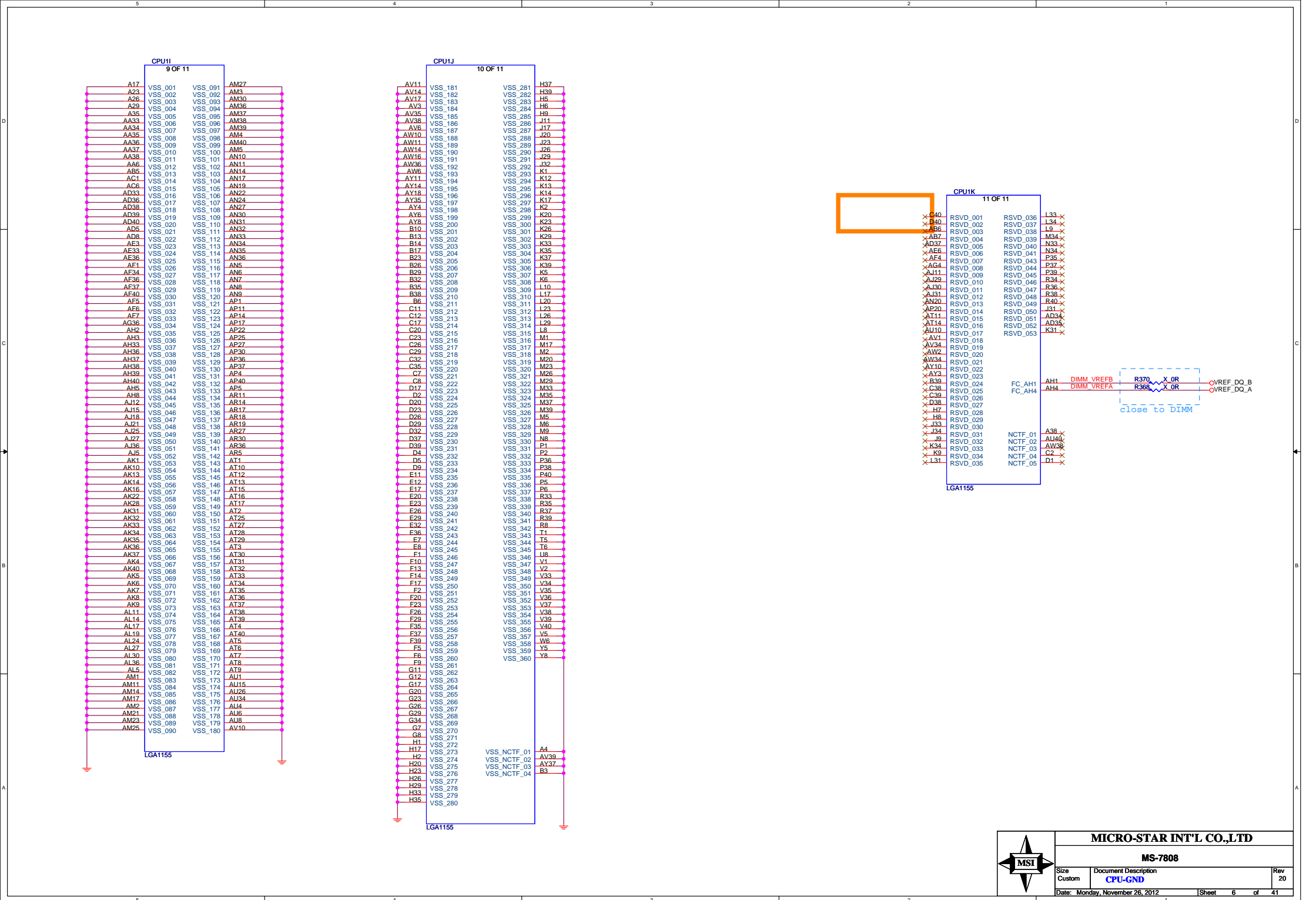
TCK/TDI/TMS TERMINATION NEAR CPU



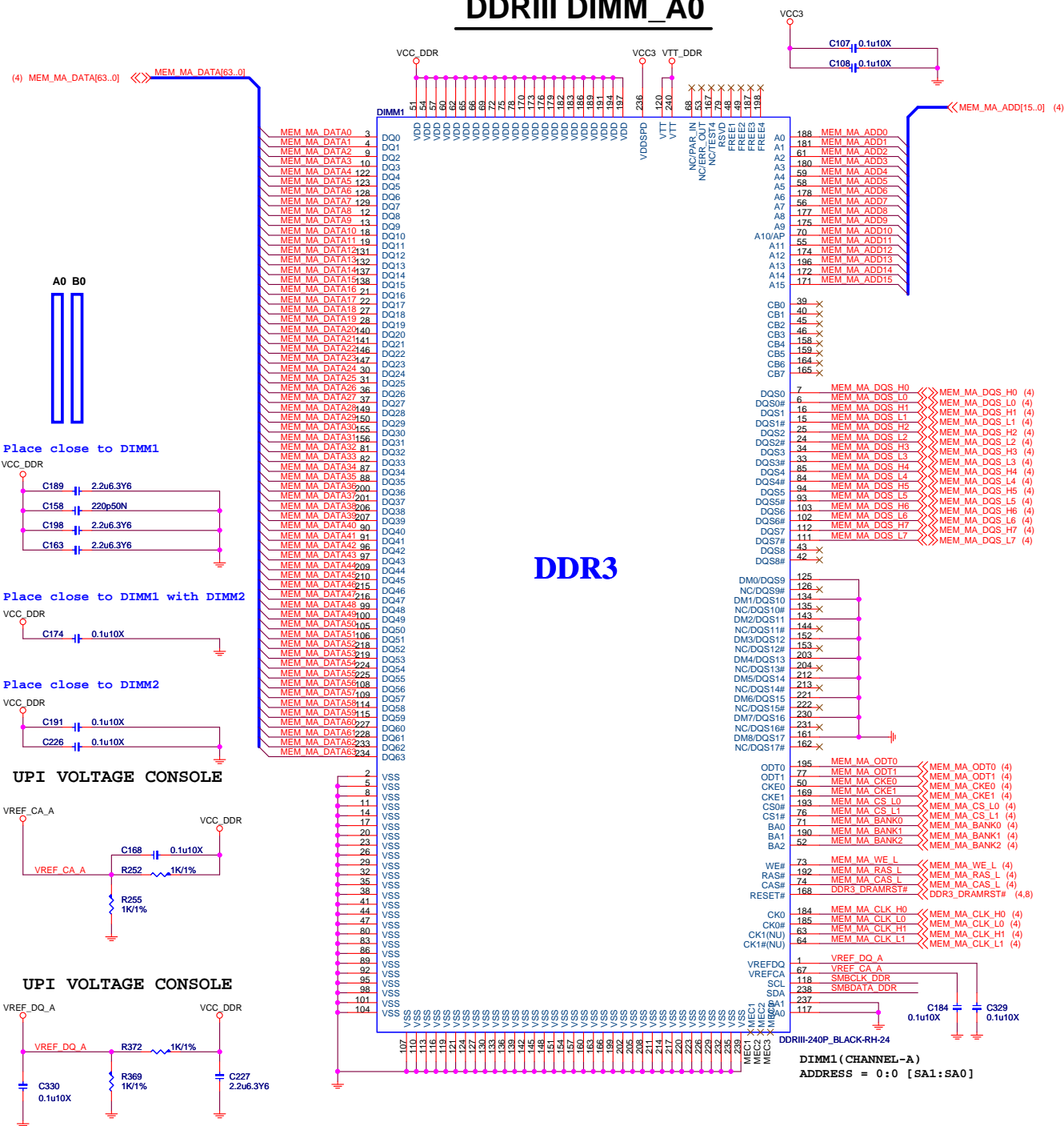
CPU_RESET#
CPURST# rise/fall time <6ns







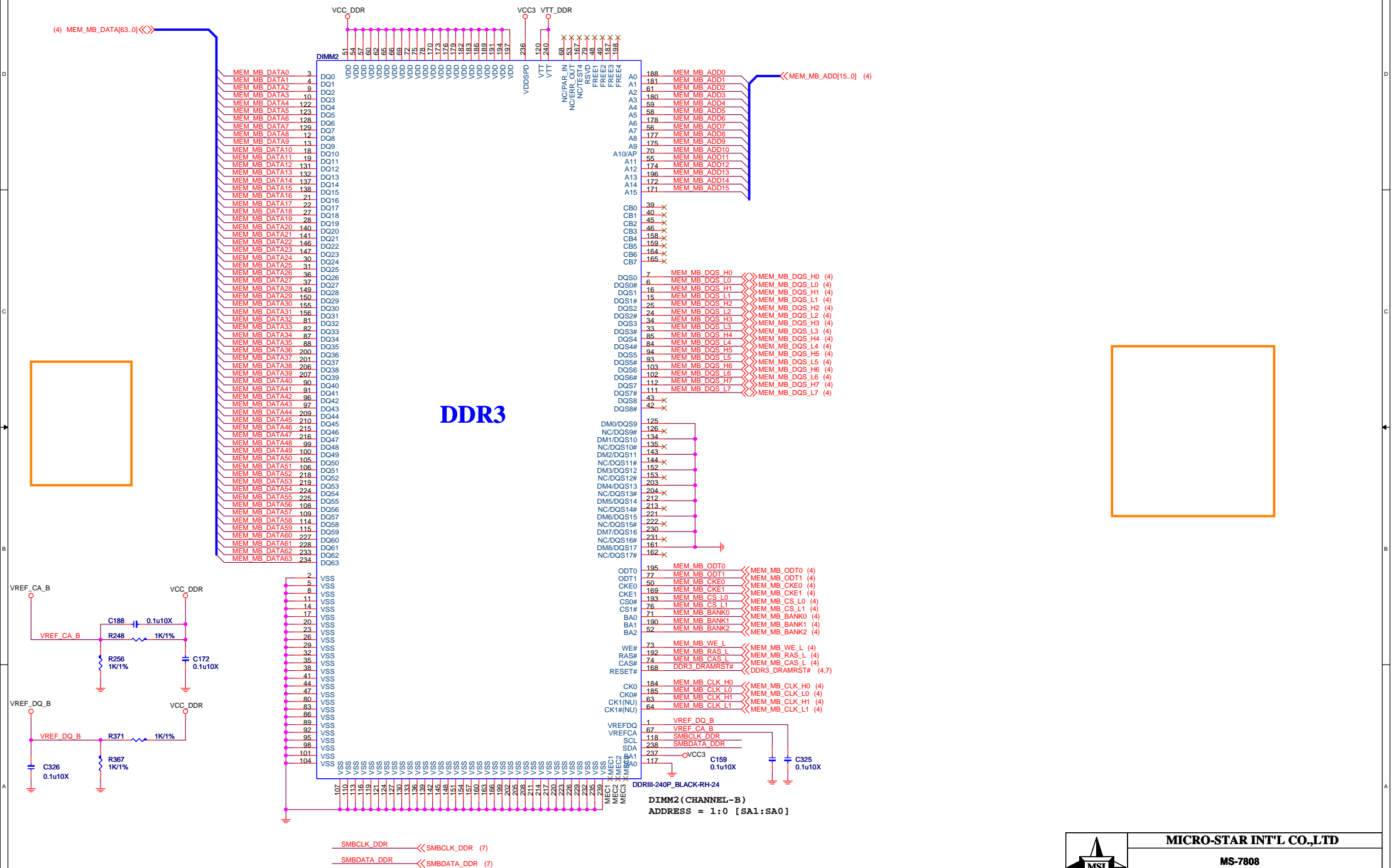
DDRIII DIMM_A0



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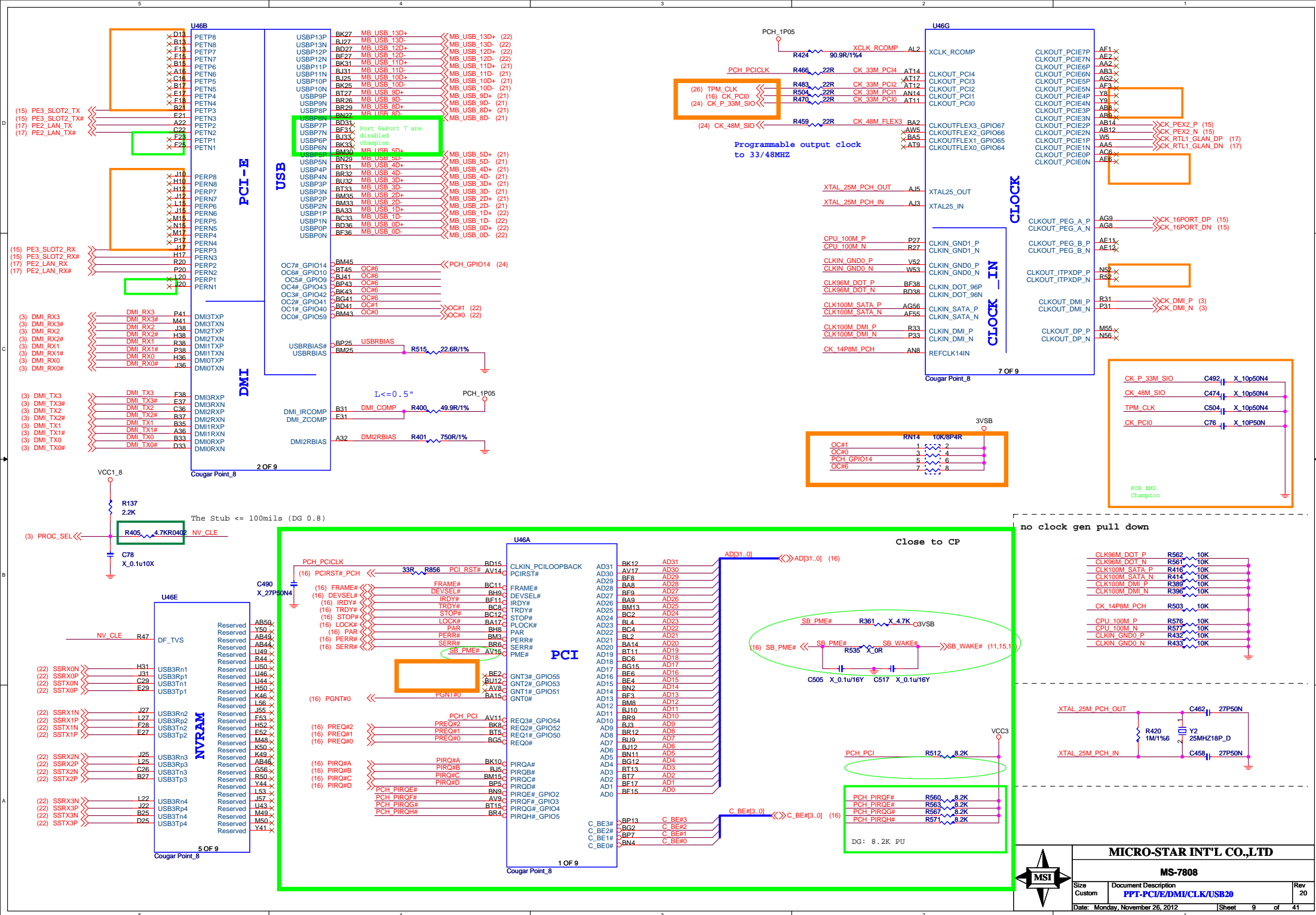
MS-7808

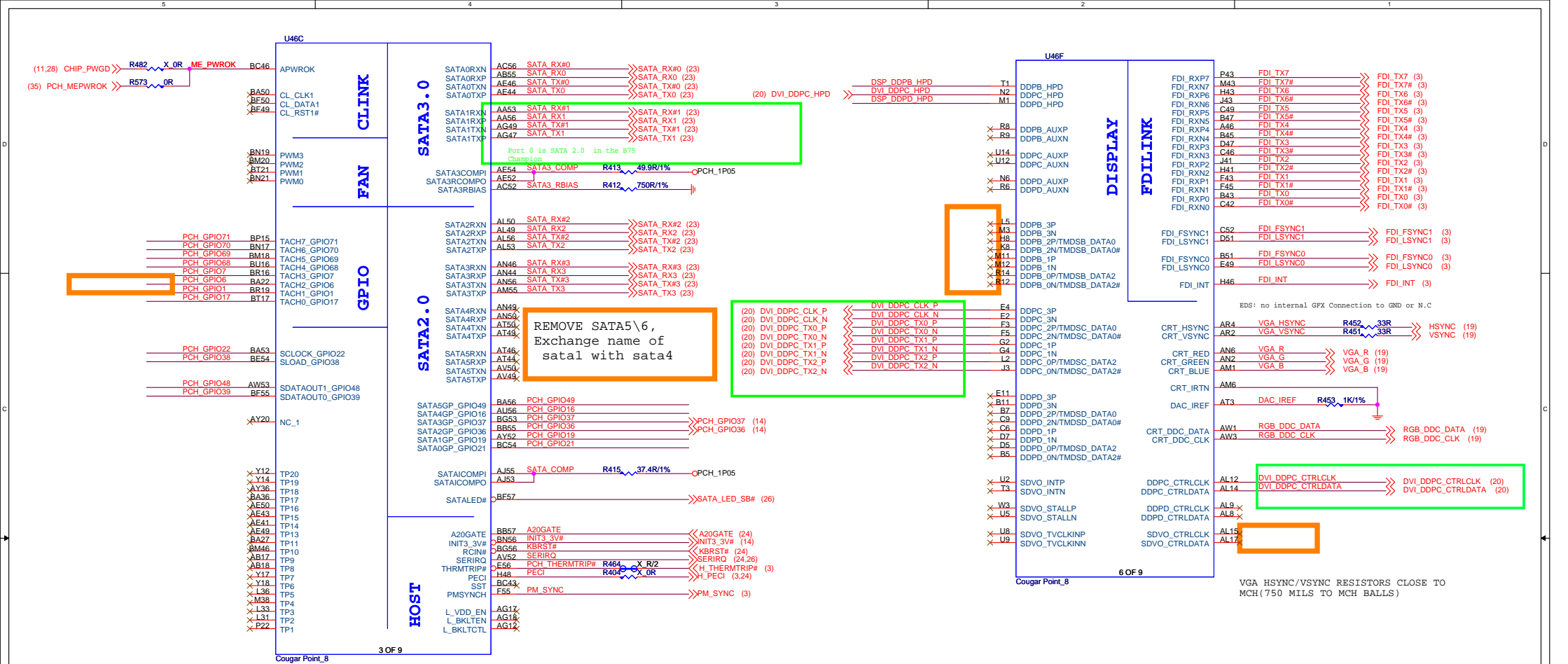
Size	Document Description	Rev
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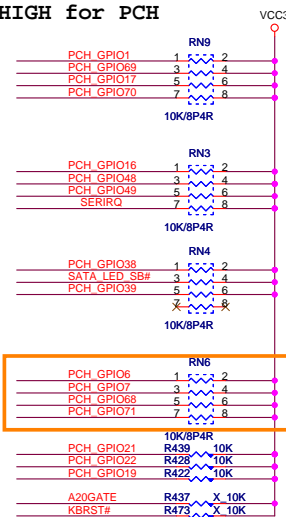
MS-7808

Size Custom	Document Description DDR3 Chane1-B DIMM3/4	Rev 20
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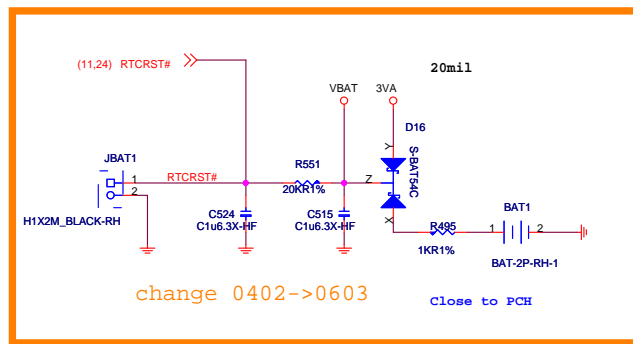
Pull HIGH for PCH



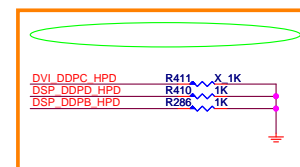
RTC and CLR_CMOS

Clear CMOS

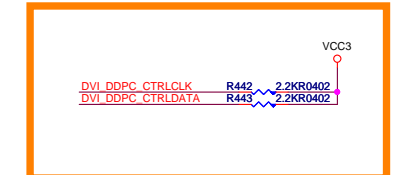
CMOS CLEAR JUMPER	
JBAT1	Clear CMOS
1-2	Clear CMOS



No Display port(pull down)



Enable VGA(CTRLCLK/DATA Pull High)



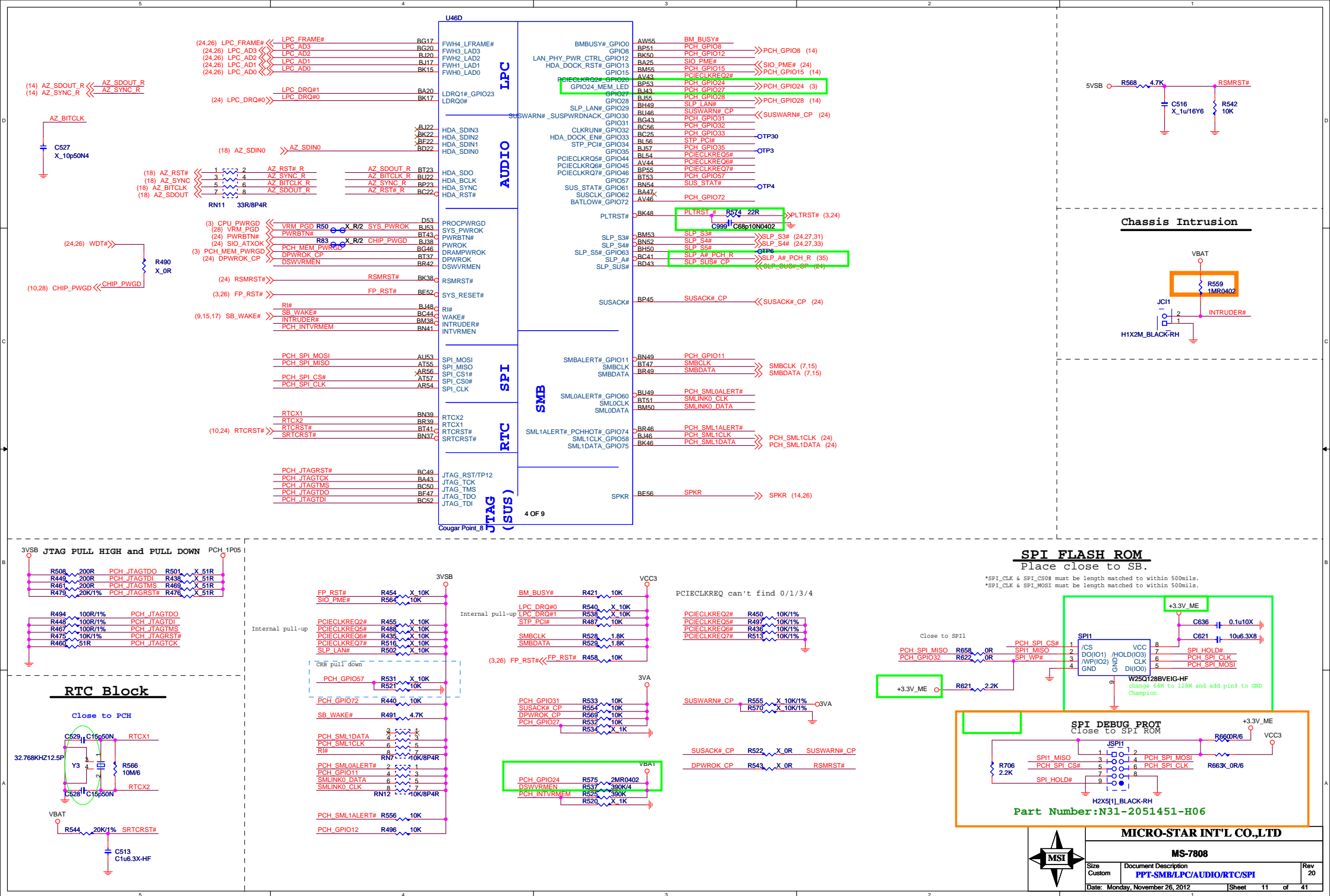
Close to PCH within 250 mils.

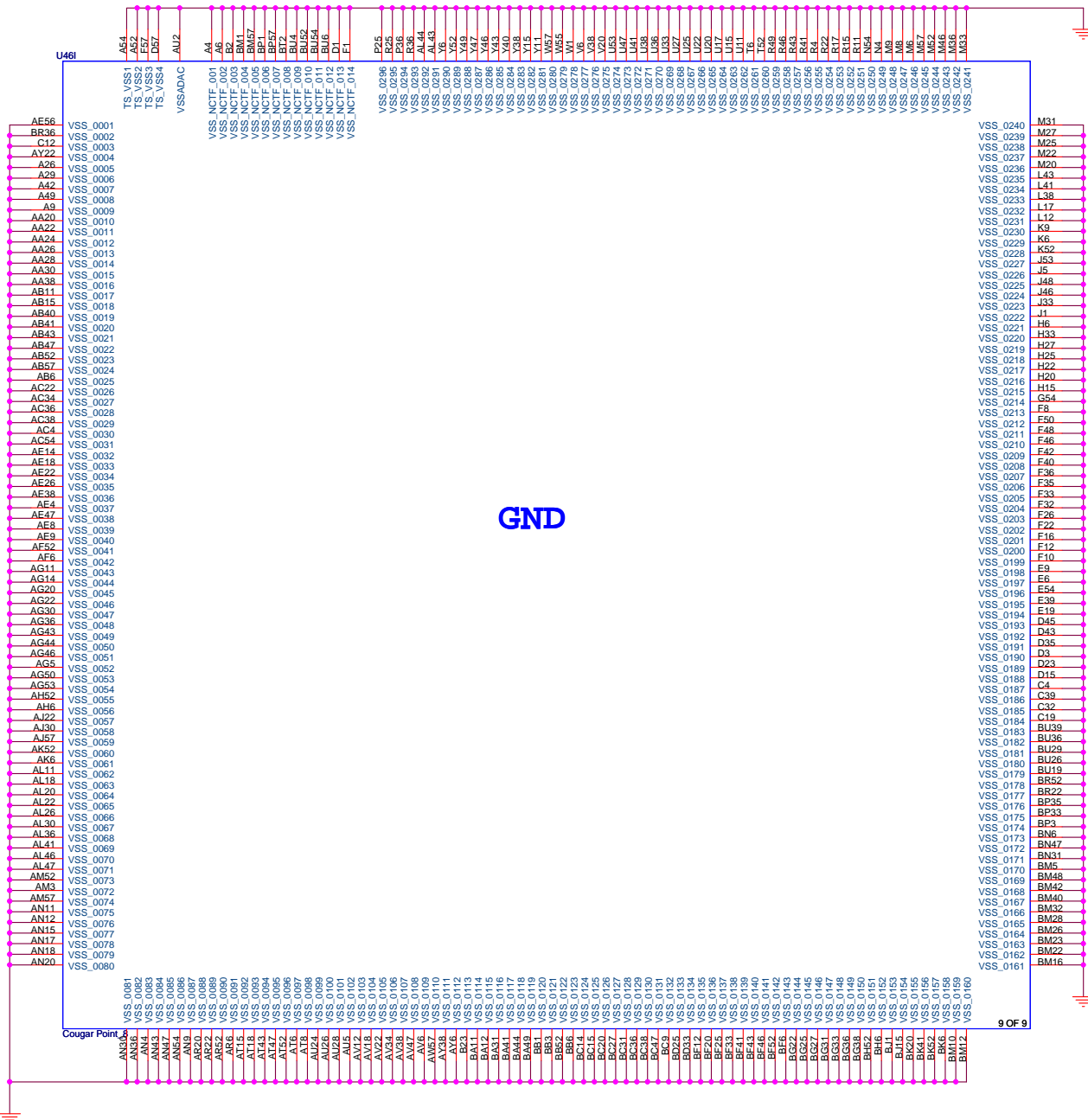


MICRO-STAR INT'L CO.,LTD

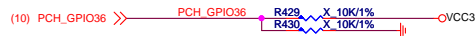
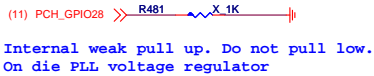
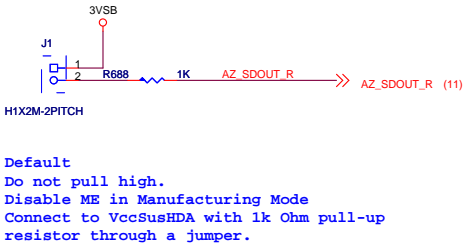
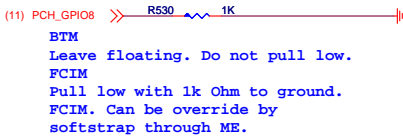
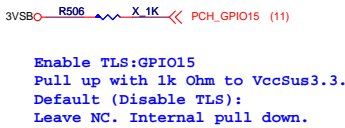
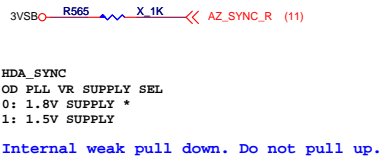
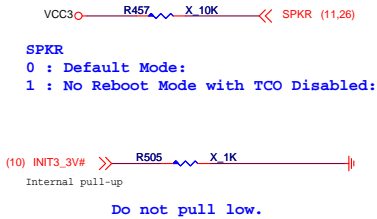
MS-7808

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Custom	PPT-SATA/HOST/GPIO/VGA/CCMOS	20
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PCH Straps

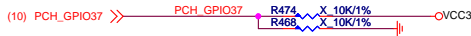


Since Pin has strap functionality that requires internal pull-down to be sampled at rising PWROK, following guidelines are required to be followed:

a) When Used as SATA2GP/SATA3GP for Mechanical Presence detect - Use a weak external pull-up (150K-200K ohms) to Vcc3_3 OR use 10K external pull-up that is enabled only after PLTRST# de-assertion.

b) When Used as GP Input (Pin HW default) - Ensure GPI is not driven high during strap sampling window

When Unused as GPIO or SATA[x]GP - Use 8.2K-10K pull-down to ground.

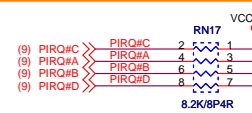
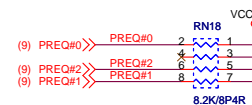
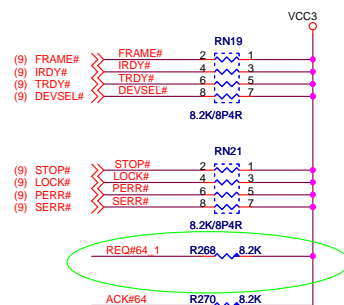
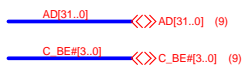
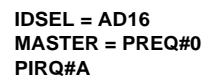


Since Pin has strap functionality that requires internal pull-down to be sampled at rising PWROK, following guidelines are required to be followed:

a) When Used as SATA2GP/SATA3GP for Mechanical Presence detect - Use a weak external pull-up (150K-200K ohms) to Vcc3_3 OR use 10K external pull-up that is enabled only after PLTRST# de-assertion.

b) When Used as GP Input (Pin HW default) - Ensure GPI is not driven high during strap sampling window

When Unused as GPIO or SATA[x]GP - Use 8.2K-10K pull-down to ground.



Remove the pull up R of PGNT
Champion

PCI slot	
+3.3Vaux	- 375mA
+3.3V	- 7.6A
+12V	- 0.5A



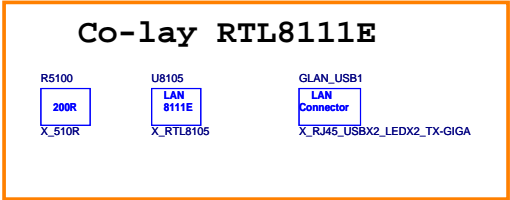
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ENSWREG:

- 1: Enable switching regulator
- 0: Disable switching regulator



MAX: 163mA

3VSB VDD33

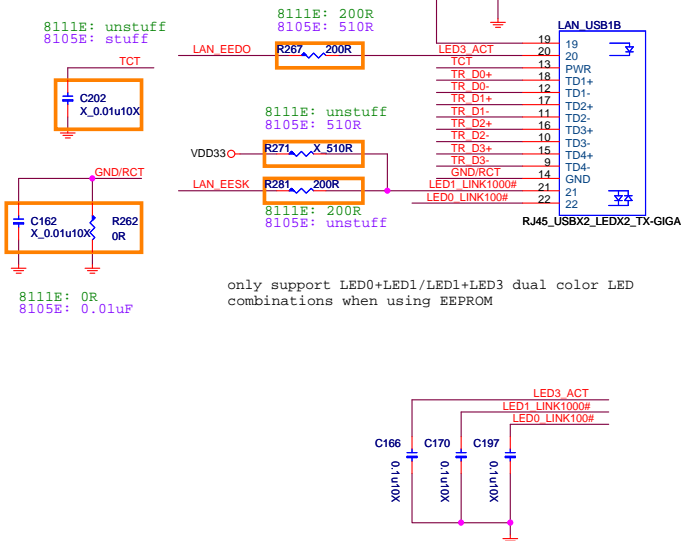
CPL X_COPPER

CPL X_COPPER

MAX: 163mA

3.3v Power on rise time : 1~100ms


	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13



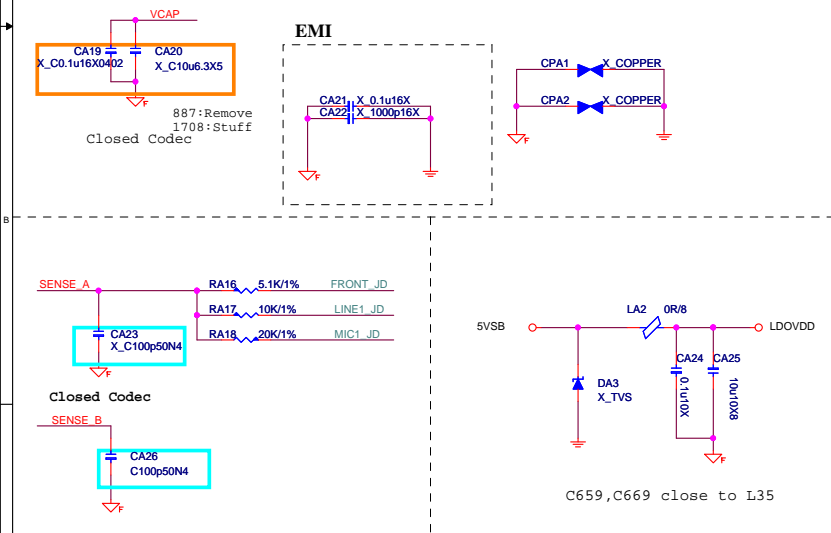
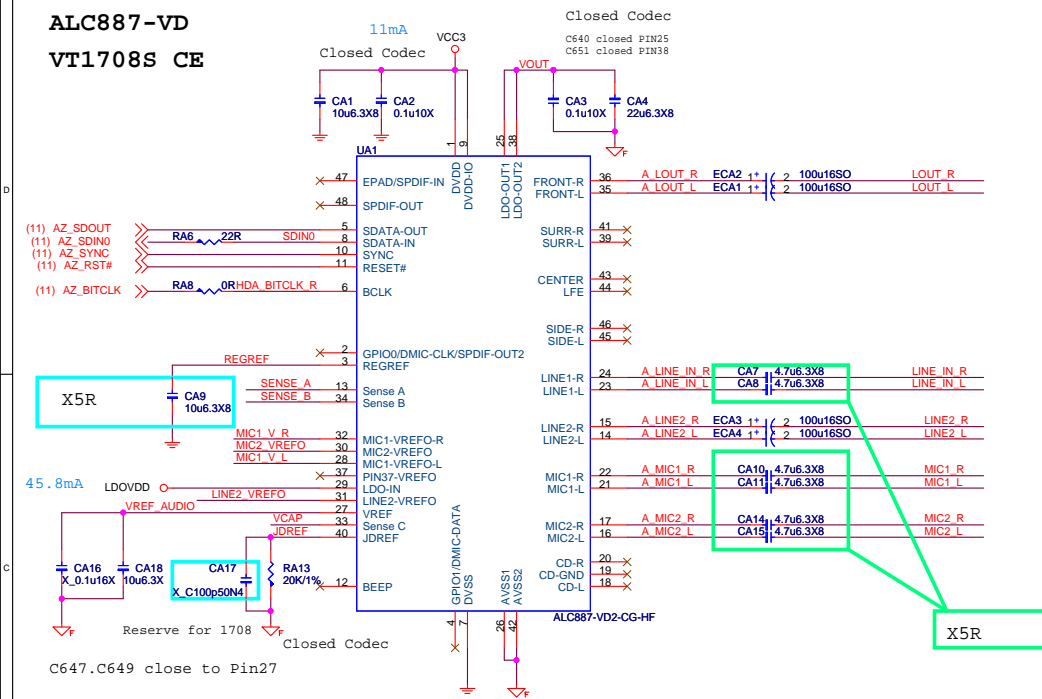
LAN Connector

Pin	Signal	Pin	Signal
19	LED3_ACT	19	PWR
18	TX0	20	TD1+
13	TR_D0+	21	TD1-
12	TR_D0-	22	TD2+
17	TR_D1+	22	TD2-
14	TR_D1-	23	TD3+
11	TR_D2+	23	TD3-
16	TR_D2-	24	TD4+
15	TR_D3+	24	TD4-
9	TR_D3-	21	GND
14	GND/RCT	22	GND
21	LED1_LINK100#	21	
22	LED0_LINK100#	22	

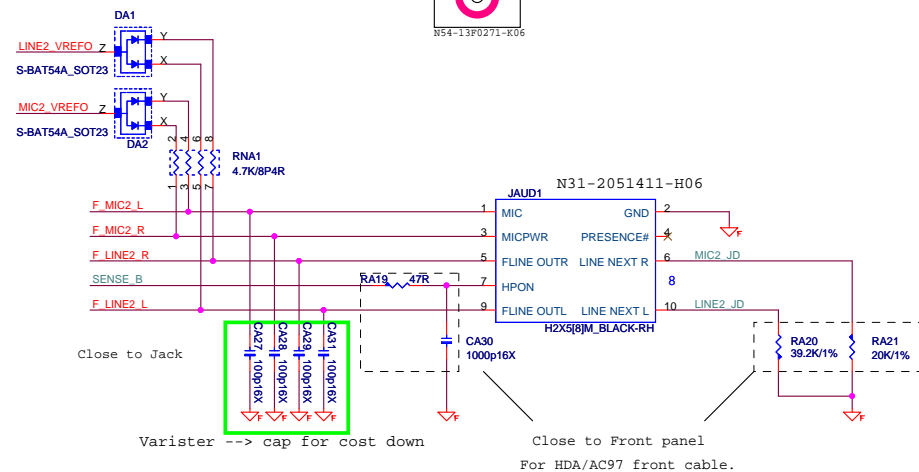
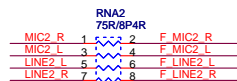
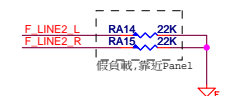
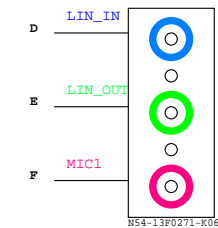
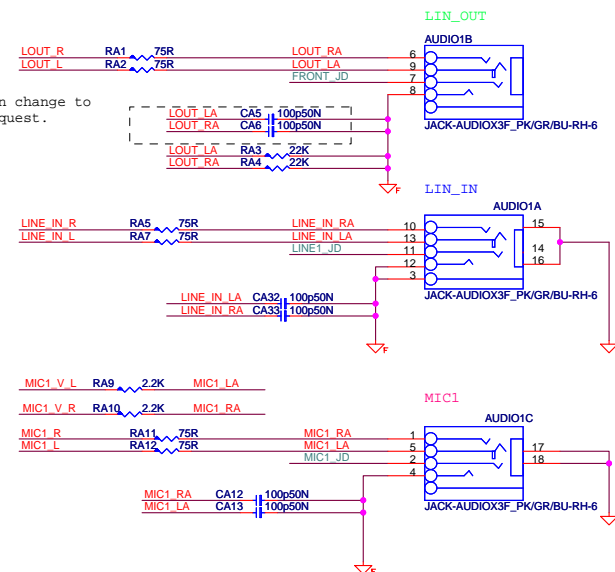
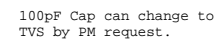
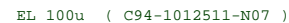
RJ45 USB2X LEDX2 TX-GIGA

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	MS-7808		
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ALC887-VD
VT1708S CE



SPDIF OUT

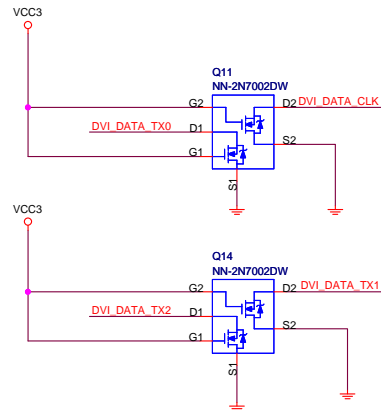
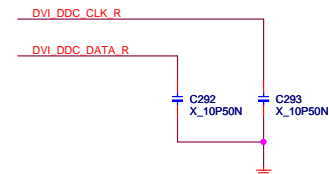
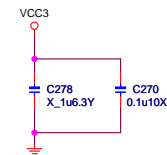
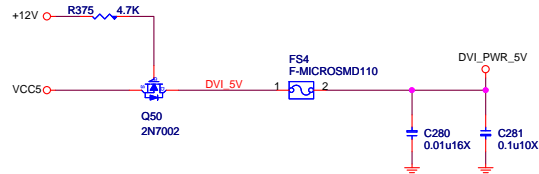
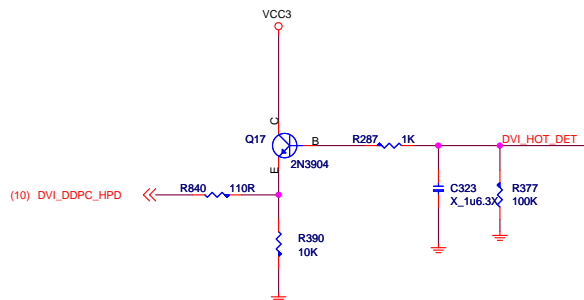
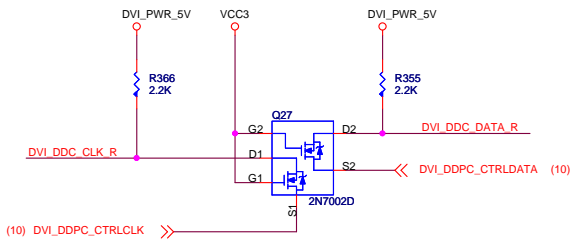
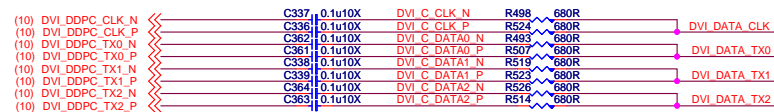


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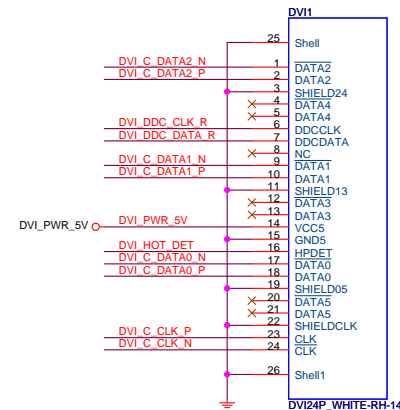
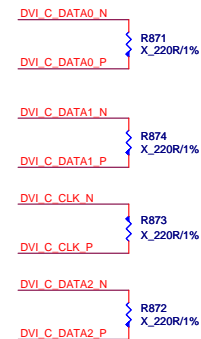
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DVI



For EMI

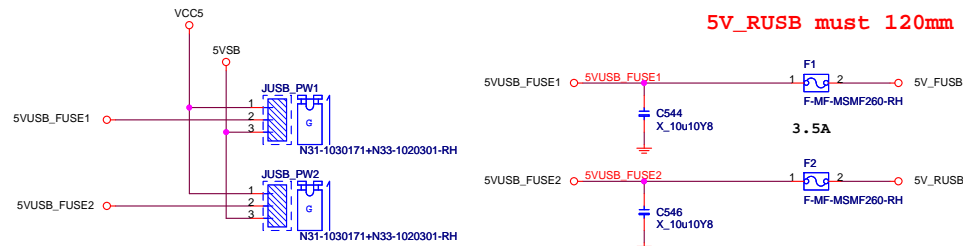


MICRO-STAR INT'L CO.,LTD

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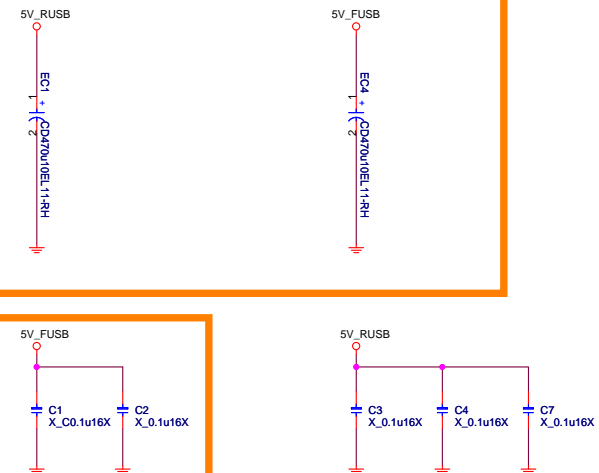
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5V_RUSB Switch

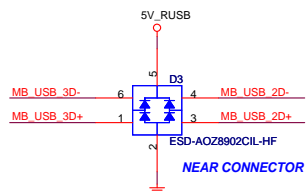
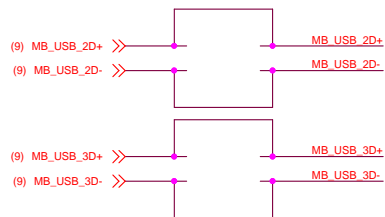


Default VCC5 (PIN1-2)

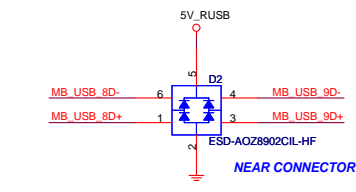
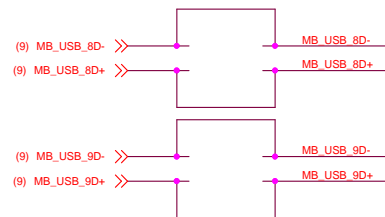
JUSB_PW1/ JUSB_PW2	BIOS Menu	Wake up support
1-2	EUP Enable	Not support
	EUP Disable	Not support
2-3	EUP Enable	Not support
	EUP Disable	support



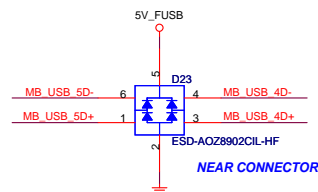
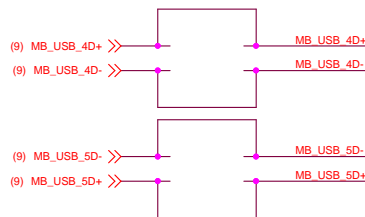
REAR USB PORT 8,9 (With LAN)



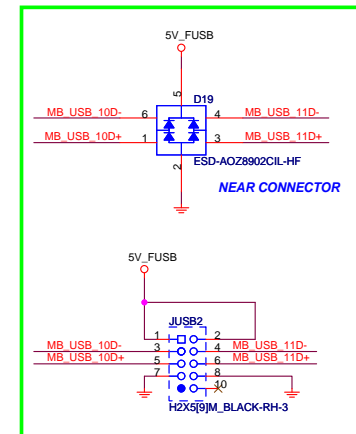
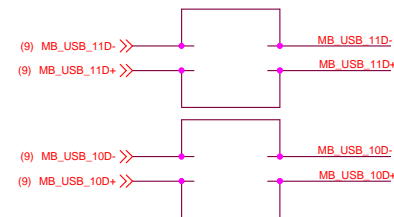
REAR USB PORT 8,9 (USB1)



FRONT USB PORT 0,1



FRONT USB PORT 8,9



Remove USB2.0 PORT 10,11
USB6&USB7
Champion



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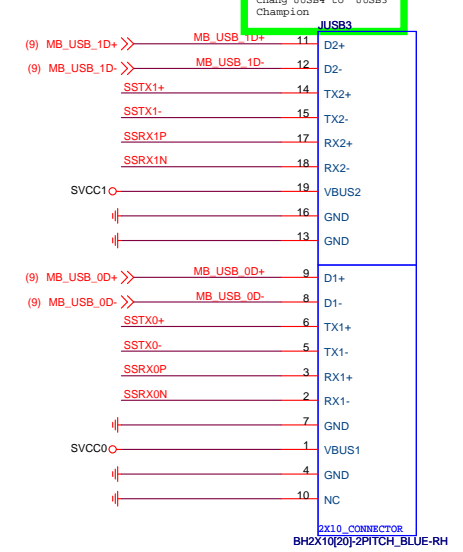
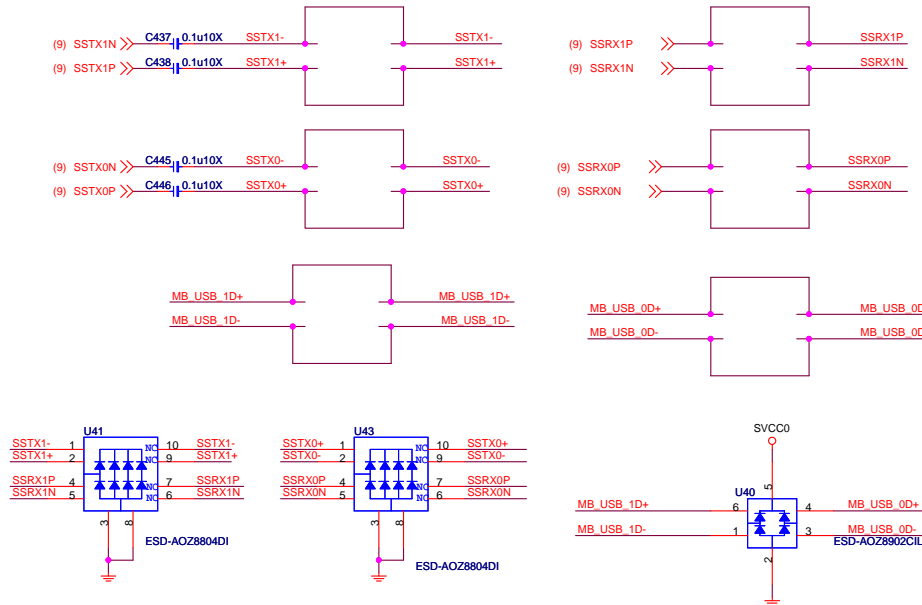
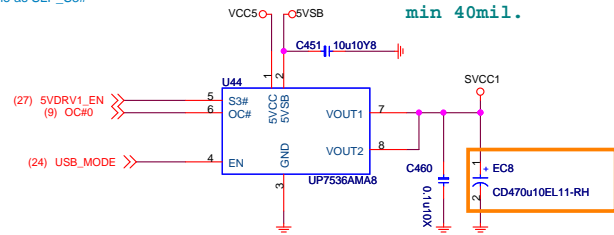
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Same as SLP_S3#



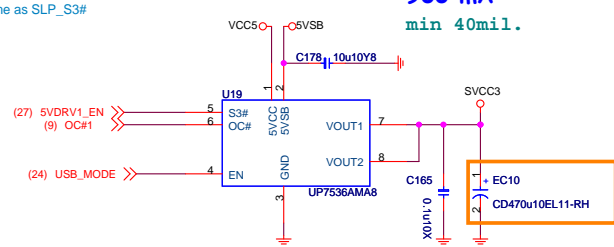
900 mA
min 40mil.



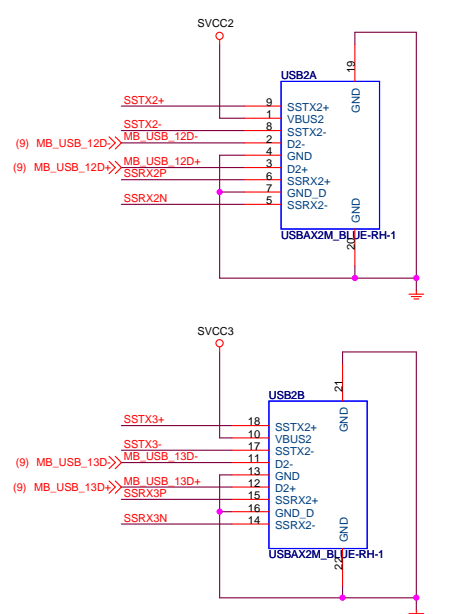
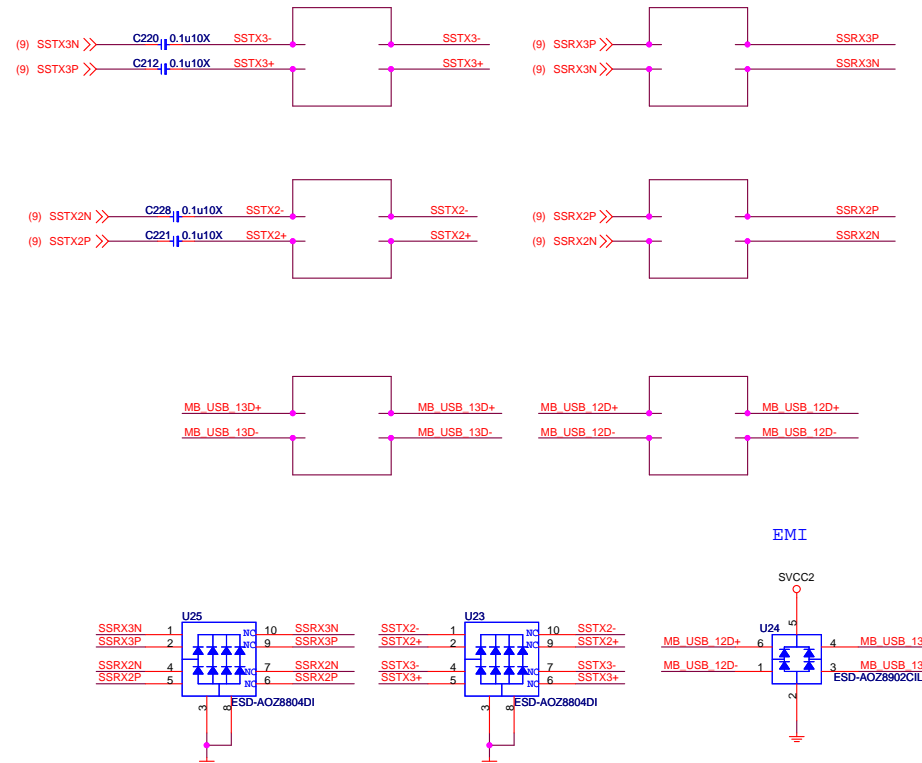
Same as SLP_S3#



900 mA
min 40mil.



MODE	G3	S4/S5	S0	S3
EUP Disable	0	0	1	1
EUP Enable	0	0	1	1



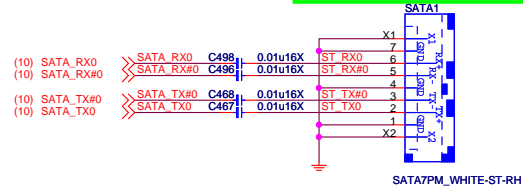
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change SATA6G PORT0,1 to SATA PORT 0

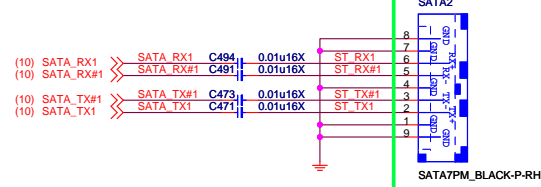
SATA 6G PORT 0

3.0 white



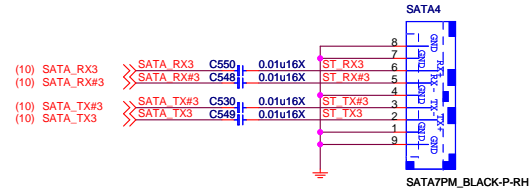
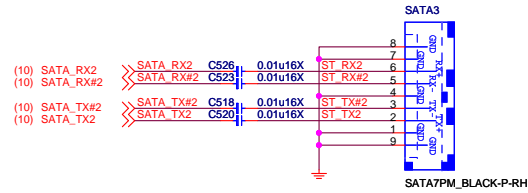
add SATA 3G PORT 1
Champion

SATA 3G PORT 1



change SATA3.0 to SATA 2.0
Champion

SATA 3G PORT 2,3



REMOVE SATA5\6 , Exchange name of satal with sata4



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FAN-CONTROL CIRCUIT

The schematic diagram illustrates a fan control circuit, labeled "FAN-CONTROL CIRCUIT". It features two main fan control sections: CPUFAN and CHAFAN, and a separate section for SYSTEM FAN1.

CPUFAN Section:

- Input: (24) SIO_CPU_FAN
- Op-Amp: LM358D_SOIC8 (X_U81A)
- MOSFET: 2N7002D (Q12)
- Resistors: R64 (2.2K), R79 (2.2K), R63 (2.2K), R62 (OR), R56 (X_10K/1%), R42 (X_3.6K/1%), R57 (4.7K), R60 (27K), R61 (10K/1%)
- Capacitors: C26 (X_0.1u16V), C5 (CD100u16EL5-RH)
- Output: CPUFAN_PWM, CPUFAN, CPU_FANTAC (24)

CHAFAN Section:

- Input: (24) SIO_SYS1_FAN
- MOSFET: NN-2N7002DW (Q10)
- Resistors: R113 (2.2K), R109 (2.2K), R84 (2.2K), R90 (4.7K), R89 (27K), R100 (10K/1%)
- Capacitors: C17 (X_0.1u16X), C16 (10u16X8)
- Output: CHAFAN_PWM, CHAFAN, SYS1_FANTAC (24)

SYSTEM FAN1 Section:

- Input: SYSFAN2
- Fan: FAN1X3
- Capacitors: C521 (X_0.1u16X), C16 (10u16X8)
- Output: EMI



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5VDIMM FOR DDR

VCC5

(24,26) ATX_PWR_OK

(11,24,31) SLP_S3#

(11,24,33) SLP_S4#

(33) SLP_S5_LCH#

R81 510R

R80 10K/1%

R103 0R

R111 X 0R

U5

S3#

S5#

MODE

GND

5VCC_DRV

5VSB_DRV

5VDRV1

5VSB

5VSBDRV1

5VCC5

5VSB

5VDRV1

R86 1K/1%6

C35 22n16X

C48 0.1u10X

C46 18n16X

C103 0.1u10X

ATX_5VSB

5VDIMM

NP-P2003ND5G

S1

S2

D

G1

G2

+12V

7501 Mode

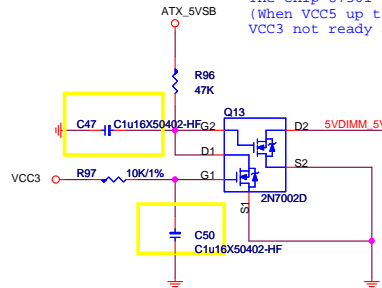
H:Support S0/S3/S5

L:Support S0/S3

```
7501 Mode
H:Support S0/S3/S5
L:Support S0/S3
```

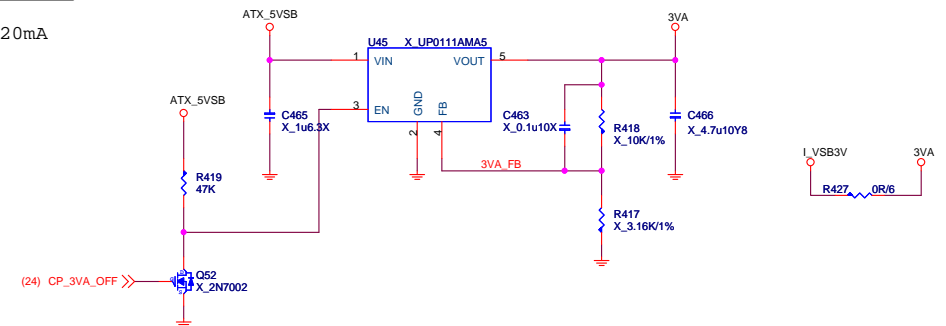
The schematic shows the power supply regulation stage. It includes an operational amplifier U29 (OP011A/MA5) configured as a non-inverting buffer, followed by another operational amplifier U30A (LM358D_SOIC8) configured as a differential amplifier. The output of U30A drives the gate of the MOSFET Q38 (N-APM3023NUC-TRG_TQ252). The output voltage is measured across the load resistor R356 and is indicated as 1.176A.

For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.



Use X7R or X5R ,VCC3 must be Powered up before 5VDRV1 in order to decrease V-drop for 3VSB(Update-2012.6.1)

20mA

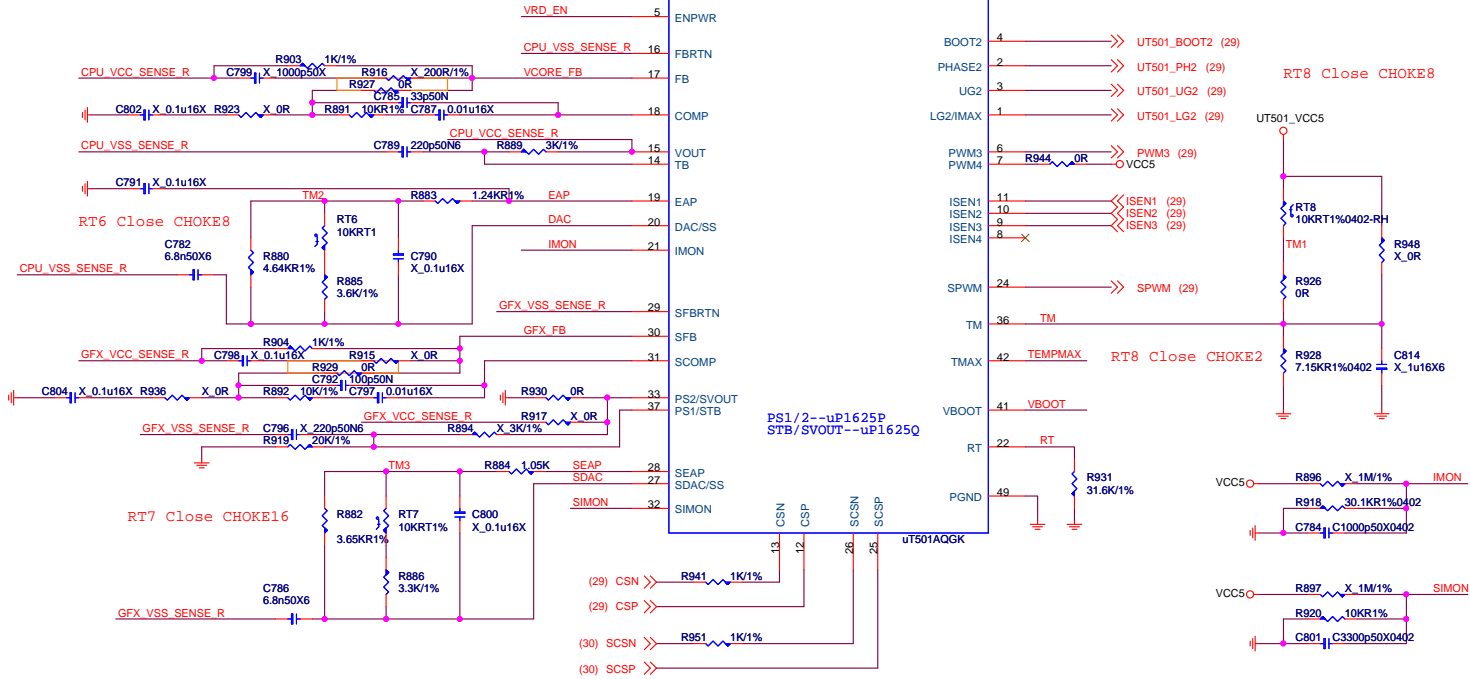
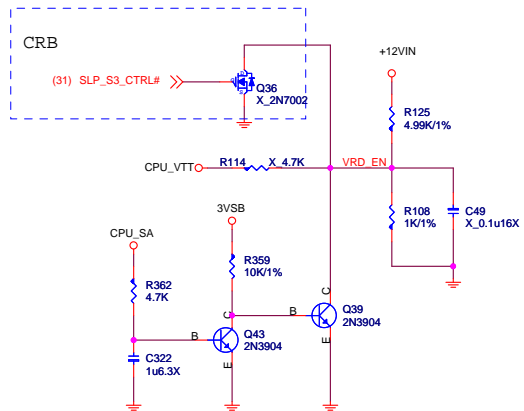
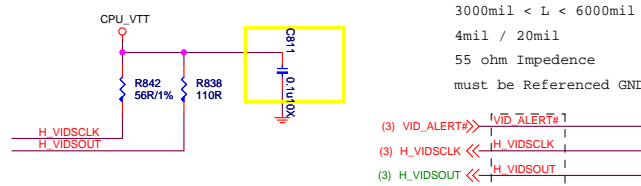
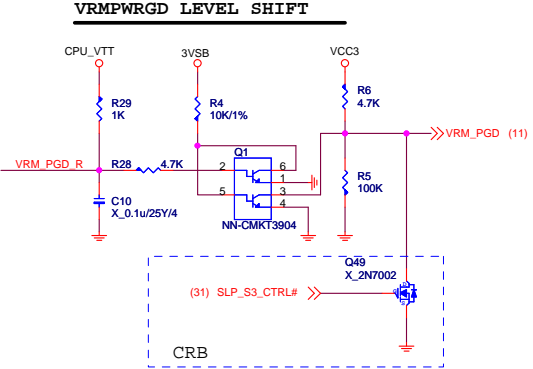


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Size Custom	Document Description ACPI controller UPI	Rev 20
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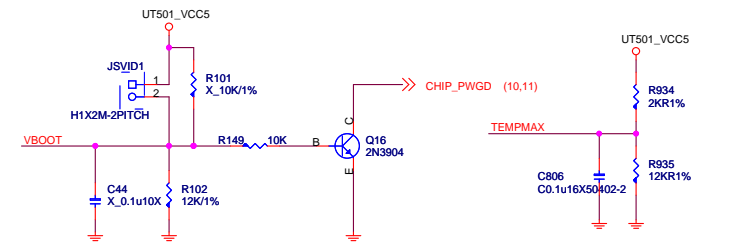
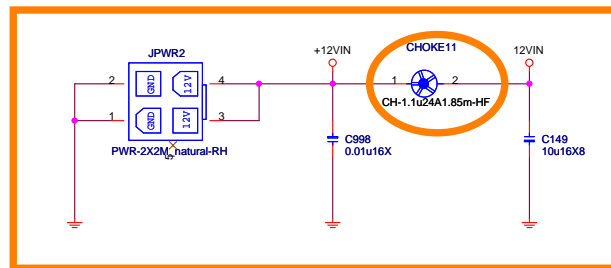
VRMPWRGD LEVEL SHIFT



UPI VOLTAGE CONSOLE

0x20:RH=10K,RL=OPEN

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%



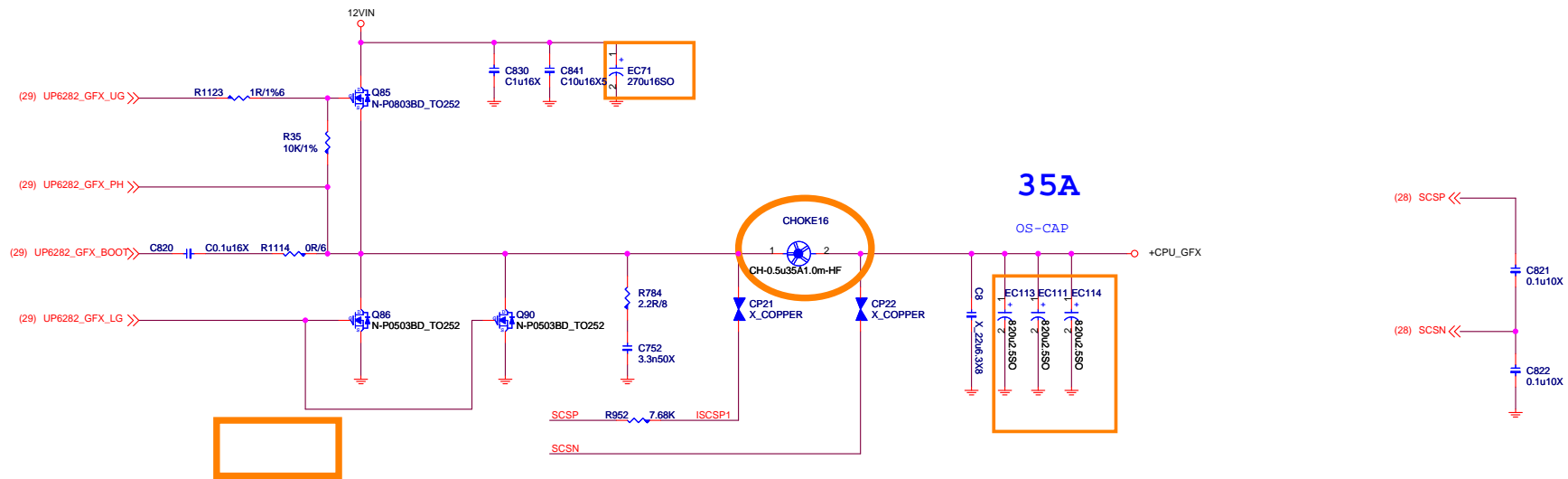
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Size	Document Description
Custom	VRD12 - PWM-UT501

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35A FOR CPU



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Size Custom	Document Description VRD12 -GPU 1-Phase MOS	Rev 20
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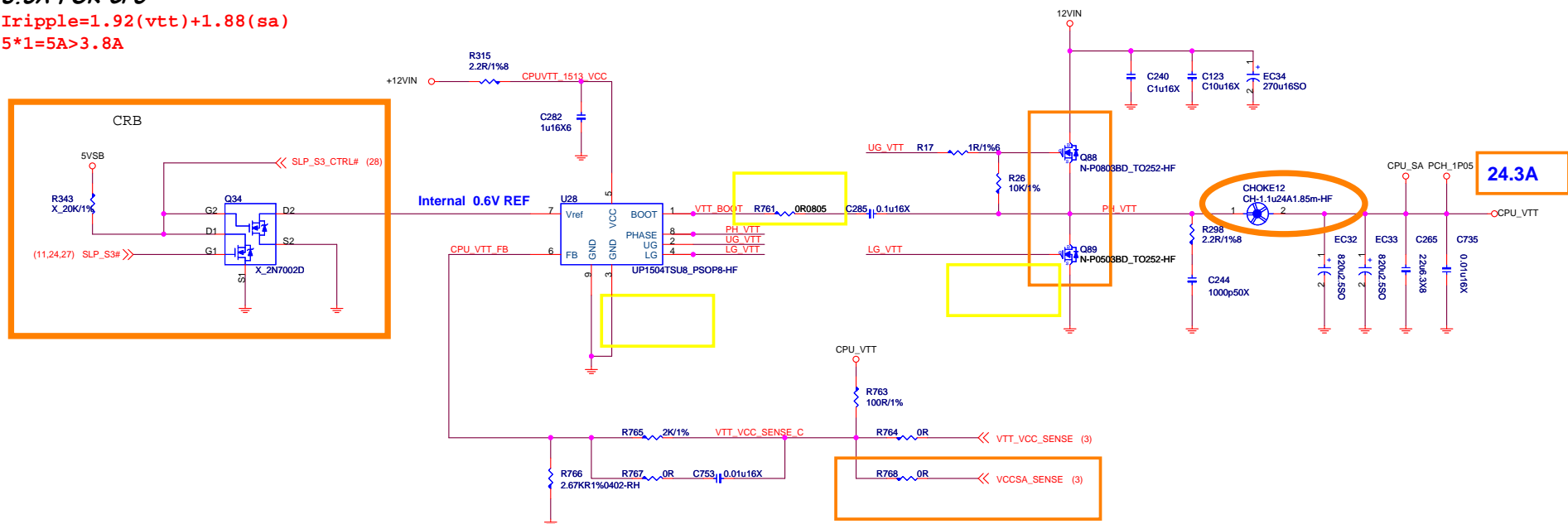
CPU_VTT:1.05/1.00 MAX 24.3A

CPU VTT 8.5A SA Core =8.8A PCH Core =7A

8.5A FOR CPU

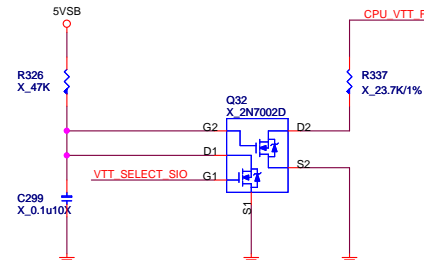
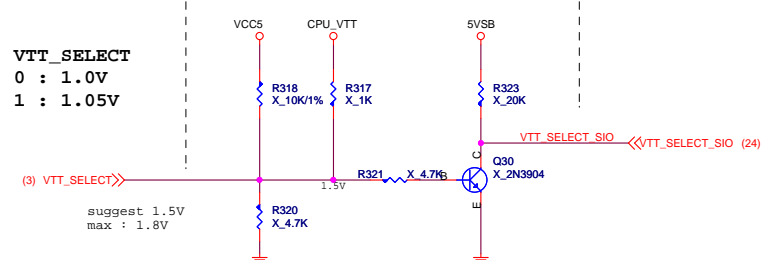
$I_{ripple} = 1.92(V_{tt}) + 1.88(sa)$

$5 \times 1 = 5A > 3.8A$



VTT_SELECT	
Low	1.0V
High	1.05V

VTT_SELECT Table	
Low	1.05V
High	1.0V



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Size	Document Description	Rev
Custom	VTT POWER- uP1513- 1Phase MOS	10
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CPU_SA:0.925/0.85

SA Core =8.8A



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Size Custom	Document Description CPU_SA OP+MOS 1-Phase	Rev 20
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DDR Power:1.5V

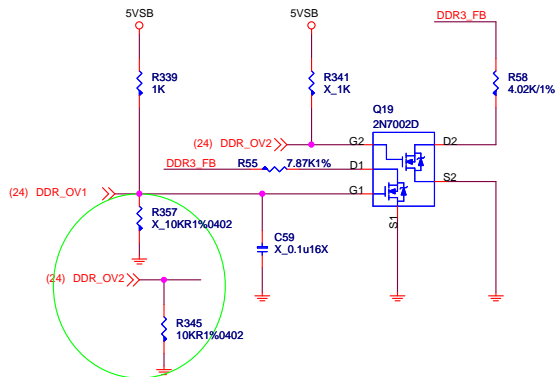
DDR3_1.5V 4.75A+5.5A+0.5A=10.75A

4.75A FOR CPU

5.5A FOR 2DIMM

0.5A FOR DDR VTT

DDR OV

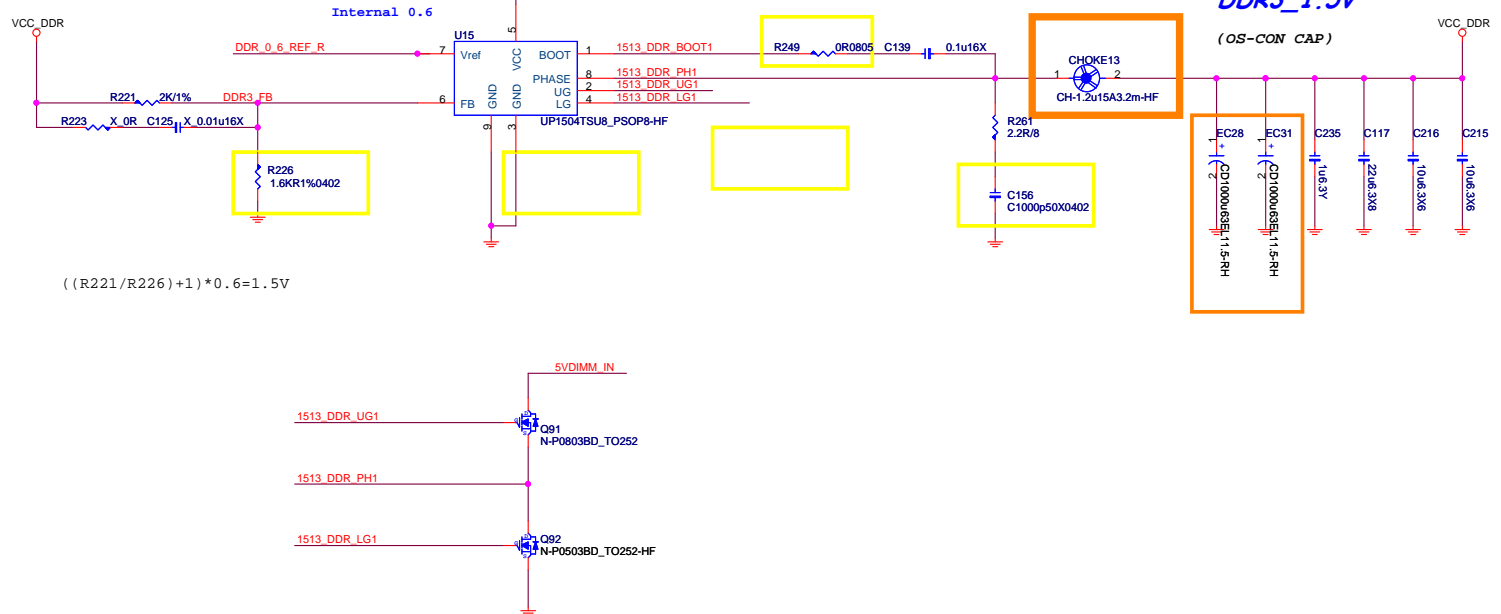


*Default 1.5V

DDR_OV	1.35V	1.5V	1.65V	1.8V
DDR_OV1	Low	High	Low	High
DDR_OV2	Low	Low	High	High

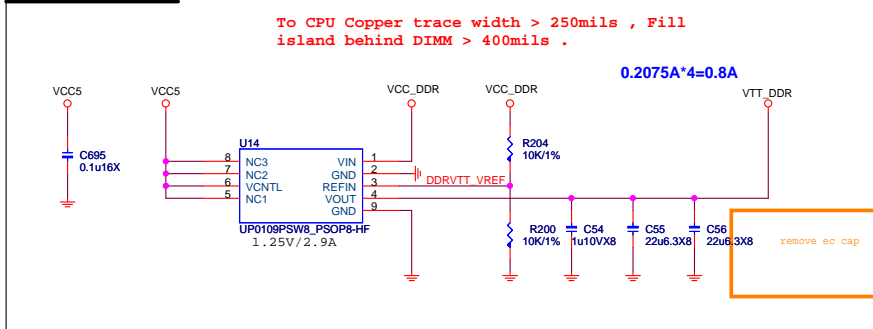
DDR_OV1 = GPIO01(S/IO)

DDR_OV2 = GPIO02(S/IO)



$$((R221/R226)+1)*0.6=1.5V$$

DDR VTT Power



To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

$$0.2075A*4=0.8A$$



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Size	Document Description	Rev
Custom	DDR Power - UP1513 1-Phase MOS	20
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P.S. Only for meet Intel power down sequence.

PCH Power:1.05V

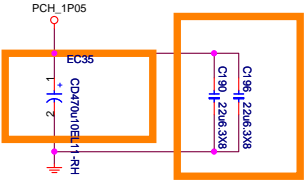
PCH Core 6.2A+0.105A+0.5A+0.08A=6.935A

6.2A FOR PCH

0.105A FOR VCCSSC

0.5A FOR VCCPLL

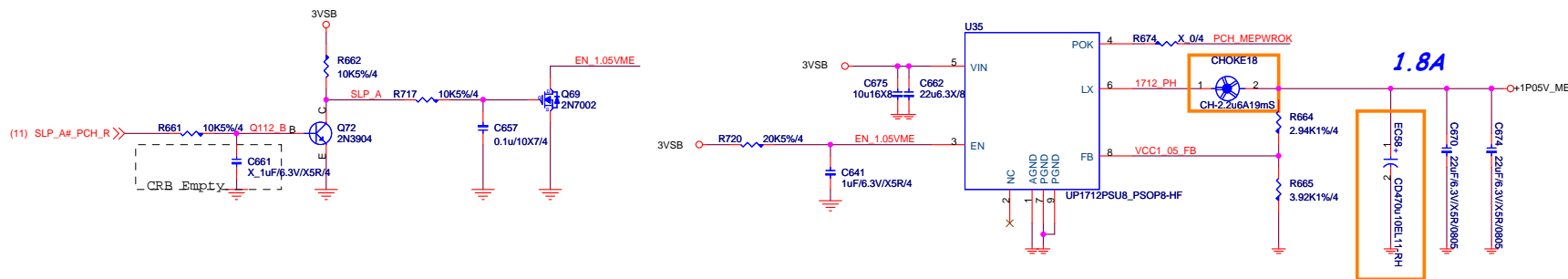
0.08A FOR VCCDMI



SLP_A

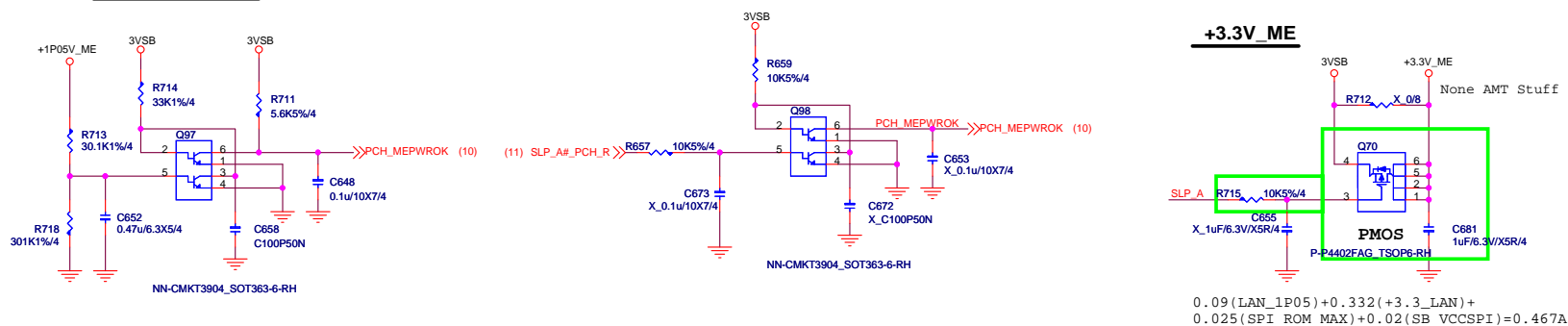
ME Power Control

+1.05V_ME(VCCIO_ME)



PCH_MEPWROK

+3.3V_ME



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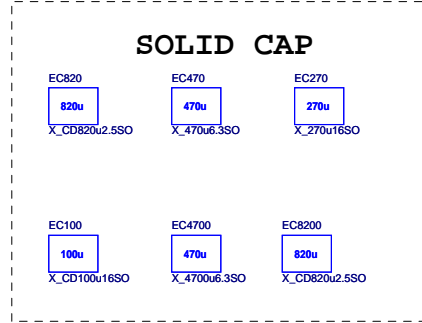
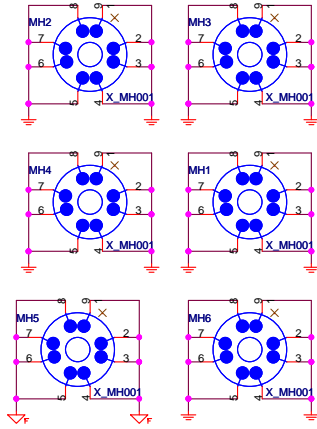
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Size Custom	Document Description ME Power - UP1712	Rev 20
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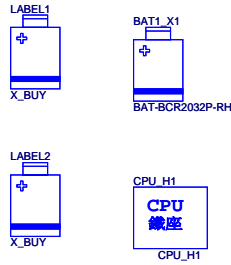
LABEL3
AMI_BIOS
LABEL_BIOS

LABEL4
AMI_BIOS
LABEL_B75MA-P33

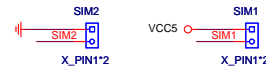


REF1
OPT
LABEL_Z77

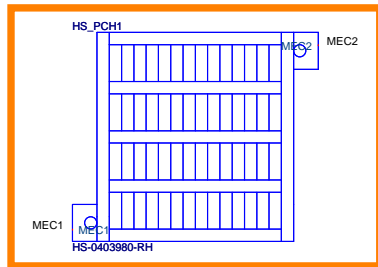
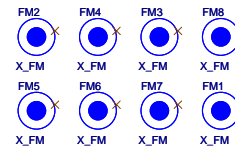
REF2
OPT
LABEL_Z77_JUC



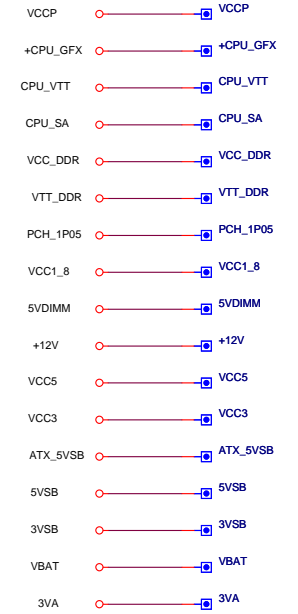
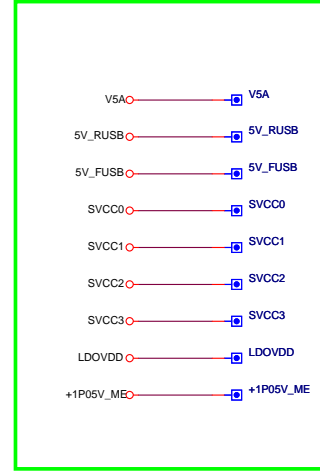
Simulation



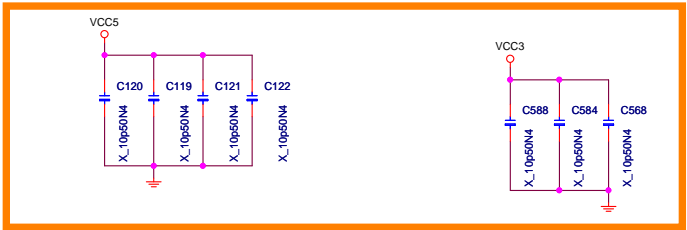
Optical Fiducial Marks-120



Voltage test point



EMI:cap. for signal return path



EMI

EMI

